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10/716,703	11/20/2003	Akira Yoshino	8070-1005	7064

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YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,703	YOSHINO, AKIRA	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 6-12* is/are rejected.

7)☒ Claim(s) *3 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-20-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 11/20/2003 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention I, **claims 1-12**, and cancellation of **claims 13-25** in the reply filed on 10/07/2004 is acknowledged.

Drawings

3. **Figures 9A through 9E, 10A, and 10B** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Similarly, **Figures 11A through 11D** are referred to as being "described in the related earlier application", therefore should also be designated by a legend such as --Prior Art-- or --Related Art-- or--Background Art.

Claim Objections

4. **Claim 3** is objected to because of the following informalities: Claim 3 recites:

"The nonvolatile semiconductor memory device according to claim 1, further comprising an oxide film formed on said insulating film on said diffusion layers, said oxide film being formed by oxidizing said first electrical conductive film".

However, it is clear that claim 2, not claim 1, cites a first electrical conductive film. Therefore, amend claim 3 to read "semiconductor memory device according to claim 2".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1 and 9** are rejected under 35 U.S.C. 102(e) as being anticipated by Chen U.S. Patent 6,784,483.

Chen discloses in the figures, particularly Figure 17, and respective portions of the specification a nonvolatile semiconductor memory device as claimed.

Referring to **claim 1**, Chen discloses a nonvolatile semiconductor memory device, comprising:

a semiconductor substrate (36) having thereon a plurality of diffusion layers for forming bit lines (21, column 8, lines 16-25) and a plurality of channel regions (no number) disposed between said adjacent diffusion layers;

an insulating film (38, "ONO stack", column 5, lines 40-45) formed on said semiconductor substrate for trapping electric charge;

an electrical conductive film (62) formed on said insulating film for forming a word line (column 8, lines 16-25),

wherein said insulating film is generally flatly formed on both said diffusion layers and said channel regions.

Referring to **claim 9**, as noted above, Chen discloses that said insulating film comprises ONO films, said ONO films being formed by depositing a silicon oxide film, subsequently depositing a silicon nitride film thereon and subsequently depositing a silicon oxide film thereon.

6. **Claims 1-2, 4, and 9-10** are rejected under 35 U.S.C. 102(e) as being anticipated by Ramsbey U.S. Patent 6,645,801.

Ramsbey discloses in Figures 1 and 3 and respective portions of the specification a nonvolatile semiconductor memory device as claimed.

Referring to **claim 1**, Ramsbey discloses a nonvolatile semiconductor memory device, comprising:

a semiconductor substrate (12) having thereon a plurality of diffusion layers for forming bit lines (26, column 3, lines 24-40) and a plurality of channel regions (no number) disposed between said adjacent diffusion layers;

an insulating film (multi-layered charge trapping ONO film 14/16/18, column 3, lines 24-40) formed on said semiconductor substrate for trapping electric charge;

an electrical conductive film (20) formed on said insulating film for forming a word line (column 3, lines 24-40),

wherein said insulating film is generally flatly formed on both said diffusion layers and said channel regions (as is evident in Figure 1).

Referring to independent **claim 4** and dependent **claim 2**, and using the same reference characters and citations as detailed above for claim 1 where applicable, Ramsbey discloses a nonvolatile semiconductor memory device, comprising:

a semiconductor substrate having thereon a plurality of diffusion layers for forming bit lines and a plurality of channel regions disposed between said adjacent diffusion layers;

an insulating film formed on said semiconductor substrate for trapping electric charge;

an electrical conductive film (20) formed on said insulating film for forming a word line,

wherein said insulating film is generally flatly formed on said channel region, and

wherein said electrical conductive film (20) comprises at least a first electrical conductive film (polysilicon or amorphous silicon layer that initially forms the word line (column 3, lines 24-27) formed on said insulating film on ("on" is interpreted broadly) said channel region and a second electrical conductive film (a saliciding metal that forms a metal silicide layer by reacting

with silicon that *initially* forms the word line, paragraph bridging columns 4 and 5) covering said first electrical conductive film.

Referring to **claims 9 and 10**, Ramsbey further discloses that said insulating film comprises ONO films (that form four rows, Fig. 1), said ONO films, as cited above, being formed by depositing a silicon oxide film, subsequently depositing a silicon nitride film thereon and subsequently depositing a silicon oxide film thereon.

7. **Claims 1-2, 4, 6, and 9-12** are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. U.S. Patent 6,524,913.

Lin discloses in Figures 2 and 3 and respective portions of the specification a nonvolatile semiconductor memory device as claimed.

Referring to **claim 1**, Lin discloses a nonvolatile semiconductor memory device, comprising:

a semiconductor substrate (200) having thereon a plurality of diffusion layers for forming bit lines (250, column 3, lines 25-35) and a plurality of channel regions (no number) disposed between said adjacent diffusion layers;

an insulating film (charge trapping ONO structure 238, column 3, lines 12-24) formed on said semiconductor substrate for trapping electric charge;

an electrical conductive film (240/254, "film" is interpreted broadly, as will be clear in the following paragraphs) formed on said insulating film for forming a word line (column 4, lines 7-15),

wherein said insulating film is generally flatly formed on both said diffusion layers and said channel regions (as is evident from the figures).

Referring to independent **claim 4** and dependent **claim 2**, and using the same reference characters and citations as detailed above for claim 1 where applicable, Lin discloses a nonvolatile semiconductor memory device, comprising:

a semiconductor substrate having thereon a plurality of diffusion layers for forming bit lines and a plurality of channel regions disposed between said adjacent diffusion layers;

an insulating film formed on said semiconductor substrate for trapping electric charge;

an electrical conductive film (240/254) formed on said insulating film for forming a word line,

wherein said insulating film is generally flatly formed on said channel region, and

wherein said electrical conductive film (240/254) comprises at least a first electrical conductive film (240) formed on said insulating film on said channel region and a second electrical conductive film (254) covering said first electrical conductive film.

Referring to **claim 6**, Lin further discloses that said insulating film (238) is formed such that the thickness of said insulating film (the thickness of ON film 210/220, Fig. 2E) is smaller on said diffusion layers (250) than the thickness thereof (of 210/220/230, Fig. 2E) on said channel regions (no number, between said adjacent diffusion layers).

Referring to **claims 9 and 10**, Lin further discloses that, and as cited above, said insulating film (238) comprises ON films (210/220, Figs. 2B and 2C), said ON films being formed by depositing a silicon oxide film and subsequently depositing a silicon nitride film thereon, or ONO films (210/220/230, Figs. 2B and 2C), said ONO films being formed by

depositing a silicon oxide film, subsequently depositing a silicon nitride film thereon and subsequently depositing a silicon oxide film thereon.

Referring to **claims 11 and 12**, Lin further discloses that said diffusion layers (buried bit lines 250) are formed by ion implantation (ion implantation 244, figure 2B and column 3, lines 25-30) after forming the charge trapping ONO layer 210/220/230 - silicon oxide/silicon nitride/silicon oxide), therefore, although not explicitly disclosed, parts of said silicon nitride film (220) of said ON films (Fig. 2C) or said ONO films (Fig. 2B) formed on said diffusion layers are transmuted by ion-implantation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 7-8 and 11-12** are rejected under 35 U.S.C. §103(a) as being unpatentable over Ramsbey.

Referring to **claims 7 and 8**, as noted above, Ramsbey discloses a nonvolatile semiconductor memory device comprising said first electrical conductive film including polycrystalline silicon or amorphous silicon and said second electrical conductive film including metal silicide. However, in the embodiment of Figures 1 and 3, Ramsbey fails to teach that the metal silicide is a refractory metal silicide. In other words, the reference fails to disclose that the metal is a refractory metal. Nevertheless, in the embodiment of Figure 5 (which discloses also a

process for forming a nonvolatile semiconductor memory device, only in more processing details but in less of a pictorial description for the final product - thus lacking the feature "generally flat" for the insulating layer, which constitute the failure of "anticipation" of a 102 rejection), the reference teaches that the metal that is used in the saliciding process to form the metal silicide comprises any suitable metal, including Ti, Ni, Co (which are refractory metals). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the nonvolatile semiconductor memory device of the embodiment of Fig. 1 using the metal material disclosed in the embodiment of Fig. 5, which metal is a refractory metal to form a refractory metal silicide, since it is generally within the skill of one in the art to select a suitable material.

Referring to **claims 11 and 12**, the step of forming the diffusion layers, which is by ion implantation or diffusion as is known in the art, takes place after the step of forming the ONO charge trapping layer (paragraph bridging columns 3 and 4), therefore parts of said silicon nitride film of said ONO films formed on said diffusion layers are transmuted by ion-implantation, if the step of forming the diffusion layers is by ion implantation. Just like selecting a suitable material, selecting a suitable step, i.e., ion implantation or diffusion in the instant case, to form diffusion layers is generally within the skill of an ordinary worker in the art and is therefore obvious. Alternately, if the step of forming the diffusion layers is by diffusion, the dopants that form the diffusion layers would also likely to transmute, or transmute to some degree, parts of the silicon nitride film of the ONO films that are formed on the diffusion layers since the dopants have to go through the parts of the silicon nitride film of the ONO films formed on the diffusion layers to reach the substrate where the diffusion layers are formed.

Allowable Subject Matter

9. Claims 3 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and in the case of claim 3, rewritten to overcome the objection noted above.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a structure for forming a nonvolatile semiconductor memory device having all exclusive limitations as recited in claims 1/2/3 (all limitation of claims 1, 2, and 3) or claims 4/5, characterized in that an oxide film formed on the diffusion layer, the oxide film being formed by oxidizing the first electrical conductive film.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
October 26, 2004